

CLAIMS

WE CLAIM:

1. An improved high-speed adaptive equalizer device comprising:
 - one or more controllable analog filters comprising:
 - one or more data signal inputs for receiving one or more data signals;
 - one or more control signal inputs for receiving one or more control signals; and
 - one or more outputs for carrying filtered data signal output signals; and
 - one or more error generators for assessing the performance of one or more of said controllable analog filters according to one or more error functions coupled to one or more of said analog filters comprising:
 - one or more inputs for receiving one or more of said filtered data signal output signals from said controllable analog filter; and
 - one or more outputs for carrying error generator output data signals.
2. The improved high-speed adaptive equalizer device of claim 1 further comprising one or more processing modules for processing said error generator output data signals creating processed data signals.
3. The improved high-speed adaptive equalizer device of claim 2 wherein one or more of said processing modules comprise one or more error acquisition blocks for applying one or more acquisition filters to one or more of said error generator output data signals thereby creating one or more processed signals coupled to one or more of said error generators comprising:
 - one or more inputs for receiving said error generator output data signals; and
 - one or more outputs for carrying processed data signals.

4. The improved high-speed adaptive equalizer device of claim 3 wherein one or more of said acquisition filters comprise an anti-aliasing filter, a noise reduction filter, a low pass filter or an integrator.

5. The improved high-speed adaptive equalizer device of claim 1 further comprising one or more equalizer controllers for controlling one or more of said controllable analog filters according to one or more algorithms comprising:

one or more inputs for receiving equalizer controller input data signals;

one or more outputs for carrying said control signals coupled to one or more of said control signal inputs.

6. The improved high-speed adaptive equalizer device of claim 1 wherein said equalizer controller input data signals comprise processed data signals or error generator output data signals.

7. The improved high-speed adaptive equalizer device of claim 1 wherein said controllable analog filter device comprises a digital, analog or hybrid device.

8. The improved high-speed adaptive equalizer device of claim 3 wherein one or more of said algorithms comprise a quasi-Newton, steepest descent or multivariate minimization algorithm.

9. The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said algorithms may be added, updated, activated, decommissioned or deleted.

10. The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said error functions may be added, updated, activated, decommissioned or deleted.

11. The improved high-speed adaptive equalizer device of claim 1 wherein said analog filter comprises one or more transversal filters, lattice filters, linear filters or non-linear filters.

12. The improved high-speed adaptive equalizer device of claim 1 wherein one or more of said data signal inputs comprise analog input, sampled analog input or digital input.

13. The improved high-speed adaptive equalizer device of claim 1 wherein one or
57 more of said control signal inputs comprise analog input or digital input.

14. The improved high-speed adaptive equalizer device of claim 1 wherein said
equalizer controller comprises one or more processing units, microprocessors, software
60 modules, firmware modules or digital devices.

15. The improved high-speed adaptive equalizer device of claim 1 wherein said
equalizer controller further comprises one or more external data outputs.

63 16. The improved high-speed adaptive equalizer device of claim 1 wherein said
equalizer controller further comprises one or more external control signal outputs.

17. The improved high-speed adaptive equalizer device of claim 1 wherein said
66 equalizer controller further comprises one or more external data inputs.

18. The improved high-speed adaptive equalizer device of claim 1 wherein said
equalizer controller further comprises one or more external control signal inputs.

69 19. The improved high-speed adaptive equalizer device of claim 1 wherein one or
more of said controllable analog filters further comprises one or more external data signal
outputs.

72 20. The improved high-speed adaptive equalizer device of claim 1 wherein one or
more of said error generators further comprises one or more external data signal outputs.

21. The improved high-speed adaptive equalizer device of claim 1 wherein one or
75 more of said error generators comprises one or more eye monitors.

22. The improved high-speed adaptive equalizer device of claim 1 wherein one or
more of said error generators comprises a clock or clock recovery system.

78 23. The improved high-speed adaptive equalizer device of claim 1 wherein one or
more of said error generators is coupled to a clock or clock recovery system.

24. The improved high-speed adaptive equalizer device of claim 1 wherein one or
81 more of said error generators comprises one or more weighting function modules.

25. The improved high-speed adaptive equalizer device of claim 1 further comprising
one or more modules comprising a capacity reporting module, a device status module, a
84 link monitor or a monitoring module.

26. The improved high-speed adaptive equalizer device of claim 1 further comprising one or more modules comprising a joint optimization module, a chromatic dispersion
87 module, a receiver gain module, a sampling phase module, a decision threshold level module or a DC offset module.

27. A method for improved high-speed adaptive equalization comprising the steps of:
90 receiving one or more data inputs at one or more controllable analog filters;
filtering said one or more data inputs according to filter coefficients to create one or more filtered data signals;
93 receiving said filtered data signals at one or more error generators; and
assessing the performance of one or more of said controllable analog filters according to one or more error functions creating one or more error generator output data
96 signals.

28. The method of claim 27 further comprising the step of providing one or more external data output signals after the step of filtering.

99 29. The method of claim 27 wherein the step of assessing the performance of one or more of said controllable analog filters further comprises applying a function to said filtered data signals comprising a normalization function or level shift function.

102 30. The method of claim 27 wherein the step of assessing the performance of one or more of said controllable analog filters further comprises applying one or more weighting functions to said error generator output data signals.

105 31. The method of claim 27 further comprising the step of processing said error generator output signals creating processed data signals.

108 32. The method of claim 31 wherein the step of processing said error generator output signals comprises the steps of:

receiving said error generator output data signals at an error acquisition module;
and

111 filtering said error generator output data signals according to one or more acquisition filters.

114 33. The method of claim 32 wherein the step of filtering said error generator output
data signals according to one or more acquisition filters comprises the step of processing
said error generator output data signals with a filter comprising an anti-aliasing filter, a
117 noise reduction filter, a low pass filter or an integrator.

34. The method of claim 32 further comprising the step of digitizing said error
generator output data signals.

120 35. The method of claim 27 further comprising the steps of:
receiving equalizer controller input data signals at an equalizer controller;
computing a new set of filter coefficients according to one or more error
123 minimization algorithms; and

controlling one or more of said controllable analog filters by adjusting said filter
coefficients to said new set of filter coefficients.

126 36. The method of claim 35 wherein said equalizer controller input data signals
comprise processed data signals or error generator output data signals.

37. The method of claim 35 further comprising the step of executing joint
129 optimization with respect to one or more external devices.

38. The method of claim 35 further comprising the step of assessing capacity, device
status or link monitor status based on said filter coefficients.

132 39. The method of claim 38 further comprising the step of reporting said capacity,
device status or link monitor status based on said filter coefficients.

40. The method of claim 27 further comprising the step of operating iteratively.

135 41. The method of claim 27 further comprising the step of initializing one or more of
said controllable analog filters to an initial setting comprising a set of said filter
coefficients based on a pass-through mode, stored values or external input.

138 42. A system for improved optical networking comprising:
an improved high-speed adaptive equalizer device coupled to an optical network
comprising:

141 one or more controllable analog filters comprising:

one or more data signal inputs for receiving one or more data signals;

one or more control signal inputs for receiving one or more control
 signals; and
 one or more outputs for carrying filtered data signal output signals;
 and
 one or more error generators for assessing the performance of one or more
 of said controllable analog filters according to one or more error functions
 coupled to one or more of said analog filters comprising:
 one or more inputs for receiving one or more of said filtered data
 signal output signals from said controllable analog filter; and
 one or more outputs for carrying error generator output data signals.

43. The system of claim 42 wherein said improved high-speed adaptive equalizer
 device further comprises one or more processing modules for processing said error
 generator output data signals creating processed data signals.

44. The system of claim 43 wherein one or more of said processing modules comprise
 one or more error acquisition blocks for applying one or more acquisition filters to one or
 more of said error generator output data signals thereby creating one or more processed
 signals coupled to one or more of said error generators comprising:
 one or more inputs for receiving said error generator output data signals;
 and
 one or more outputs for carrying processed data signals.

45. The improved high-speed adaptive equalizer device of claim 44 wherein one or
 more of said acquisition filters comprise an anti-aliasing filter, a noise reduction filter, a
 low pass filter or an integrator.

46. The system of claim 42 wherein said improved high-speed adaptive equalizer
 device further comprises one or more equalizer controllers for controlling one or more of
 said controllable analog filters according to one or more algorithms comprising:
 one or more inputs for receiving equalizer controller input data signals;
 one or more outputs for carrying said control signals coupled to one or
 more of said control signal inputs.

47. The system of claim 42 wherein said equalizer controller input data signals comprise processed data signals or error generator output data signals.

174 48. The system of claim 42 wherein said controllable analog filter device comprises a digital, analog or hybrid device.

49. The system of claim 44 wherein one or more of said algorithms comprise a quasi-
177 Newton, steepest descent or multivariate minimization algorithm.

50. The system of claim 42 wherein one or more of said algorithms may be added, updated, activated, decommissioned or deleted.

180 51. The system of claim 42 wherein one or more of said error functions may be added, updated, activated, decommissioned or deleted.

52. The system of claim 42 wherein said analog filter comprises one or more
183 transversal filters, lattice filters, linear filters or non-linear filters.

53. The system of claim 42 wherein one or more of said data signal inputs comprise analog input, sampled analog input or digital input.

186 54. The system of claim 42 wherein one or more of said control signal inputs comprise analog input or digital input.

55. The system of claim 42 wherein said equalizer controller comprises one or more
189 processing units, microprocessors, software modules, firmware modules or digital devices.

56. The system of claim 42 wherein said equalizer controller further comprises one or
192 more external data outputs.

57. The system of claim 42 wherein said equalizer controller further comprises one or more external control signal outputs.

195 58. The system of claim 42 wherein said equalizer controller further comprises one or more external data inputs.

59. The system of claim 42 wherein said equalizer controller further comprises one or
198 more external control signal inputs.

60. The system of claim 42 wherein one or more of said controllable analog filters further comprises one or more external data signal outputs.

- 201 61. The system of claim 42 wherein one or more of said error generators further
comprises one or more external data signal outputs.
- 204 62. The system of claim 42 wherein one or more of said error generators comprises
one or more eye monitors.
63. The system of claim 42 wherein one or more of said error generators comprises a
clock or clock recovery system.
- 207 64. The system of claim 42 wherein one or more of said error generators is coupled to
a clock or clock recovery system.
- 210 65. The system of claim 42 wherein one or more of said error generators comprises
one or more weighting function modules.
- 213 66. The system of claim 42 wherein said improved high-speed adaptive equalizer
device further comprises one or more modules comprising a capacity reporting module, a
device status module, a link monitor or a monitoring module.
- 216 67. The system of claim 42 wherein said improved high-speed adaptive equalizer
device further comprises one or more modules comprising a joint optimization module, a
chromatic dispersion module, a receiver gain module, a sampling phase module, a
decision threshold level module or a DC offset module.

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